User Manual

PyrIQ Interface Description

Applicable for Engineering Samples

Engineering samples are manufactured for purposes of research and development. Characteristic values mentioned in the technical description included are for guidance only and may not be used as guaranteed values. InfraTec reserves the right to change these specifications at any time without notification.

Revision: Rev 02, February 2024

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1 Introduction

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This manual has been prepared with due care. Nevertheless, errors and omissions cannot be completely excluded.

Further developments in the sense of technical progress are reserved.

No liability is assumed for damages resulting from non-observance of the information contained in this manual.

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2 General Description

A key element of InfraTec detectors with digital interface is an application-specific integrated circuit (ASIC). This ASIC enables complete flexibility in the configuration of the detector parameters and thus variable signal processing. In addition, it offers improved electromagnetic compatibility (EMC), as the entire signal conversion from the amplification in the analog front-end to the digitalization is spatially concentrated and shielded. The ASIC offers a wide range of further benefits.

It is equipped with a clock pin to synchronise the IR-source and the detector clock. This means that a time signal with a highly precise sampling rate can be generated. An additional, special feature is the „fast recovery after saturation“. This function detects saturation events due to a defective operating status and automatically resets the analog input stage.

The ASIC converts the analog signal with a resolution of 16 bit directly into a digital signal. The signals can be filtered and strengthened in multiple adjustable stages. The analog input stage of the ASIC acts like a transimpedance amplifier. The basic function principle is outlined in Figure 1. Eventually, users receive a digital measurement signal, which can be read out via a standard communication interface (I^2C) and processed immediately without further conditioning steps.

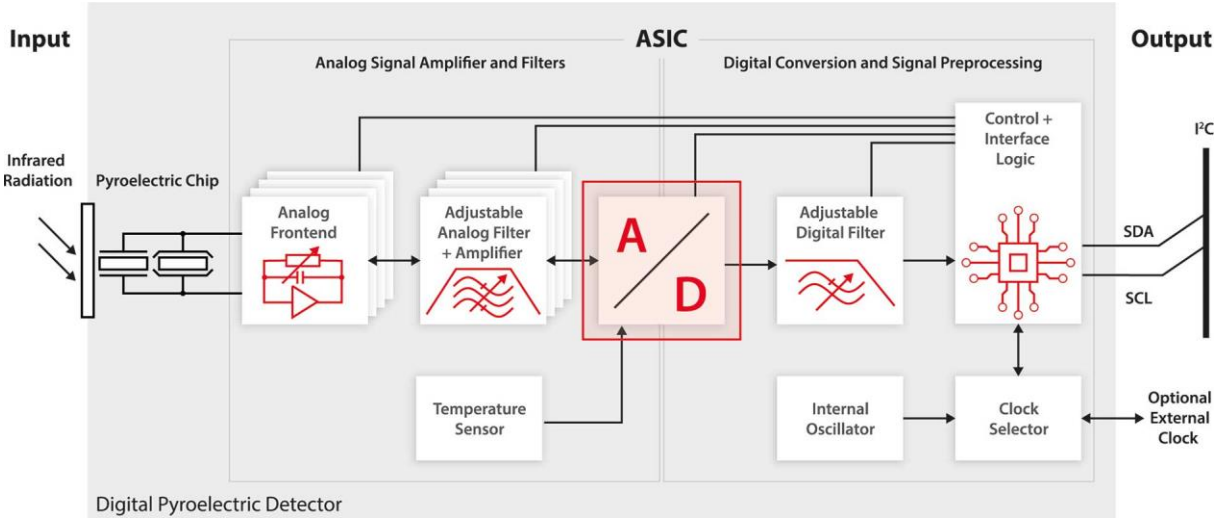


Figure 1: Schematic working principle of ASIC

A detailed description of the different function blocks of the ASIC is given in chapter 4. Here is a summary of the main features of InfraTec's detector family with digital interface:

- Low noise transimpedance amplifier in the analog front-end,
- Programmable feedback network (resistance: 2 GΩ … 1 TΩ; capacitance: 50 fF … 6.4 pF),
- Programmable low pass and high pass filters,
- ADC with 16 bit resolution at 1 kHz sampling frequency,
- I^2C communication interface,
- Detector operates with power supply range 1.75 V…3.6 V,
- Interrupt generator and controller,
- Temperature sensor.

3 Technical Requirements

3.1 Absolute Maximum Ratings

Parameter	Rating		Unit
	Min	Max	
Power Supply Voltage V_{CC}	-0.3	3.6	V
All inputs (Analog)	-0.3	V_{CC} + 0.3	V
All inputs (Digital)	-0.3	V_{CC} + 0.3	V
Digital input / output clamping value		100	mA
Operating Temperature Range	-45	85	°C
ESD HBM Protection on input		400	V
ESD HBM Protection on all pin except input		2	kV

3.2 Electrical Characteristics

Parameter	Test Condition / Comment	Tolerance	Min	Typ	Max	Unit
Power supply voltages and current						
Power supply voltage V_{CC}			1.75	3.3	3.6	V
Operation mode current	1k sample/s, 4 channels active			200		µA
Operation mode current	1k sample/s, 1 channel active			70		µA
Power down mode	Oscillator off and all input channels deactivated		0.9	2**	10*	µA
Digital input and output						
High level input voltage V_{IH}	V_{CC}=3.3 V		2		3.6	V
Low level input voltage V_{IL}	V_{CC}=3.3 V		-0.3		0.8	V
High level output voltage V_{OH}			2.4			V
Low level output voltage V_{OL}					0.4	V
Input leakage current I_{leak}					1000	pA
Input capacitance					5	pF
Communication						
I^2C clock rate				400	1000	kHz
I^2C input voltage level high			1.2			V
I^2C input voltage level low					0.6	V
Analog section						
Feedback capacitance	8 steps, chapter 4.2.1 & 4.4.9.2, sys clock 32 kHz	±10%	50		6400	fF
Feedback resistance	10 steps, chapter 4.2.1 & 4.4.9.2, sys clock 32 kHz	±10%	2		1000	GΩ
High pass bandwidth	4 steps, chapter 4.2.2 & 4.4.9.2, sys clock 32 kHz	±10%	0.5		4	Hz
Low pass bandwidth	Chapter 4.2.2, sys clock 32 kHz	±10%		200		Hz
Temperature sensor						
Resolution	Chapter 4.2.4	±1 K ***		0.012		K/digit
ADC						
Resolution				16		bit
Effective resolution (ENOB)	Exclude analog front-end			15		bit
Least significant bit voltage (U_{LSB})				29.42		µV
Digital section						
Low pass bandwidth	4 steps, chapter 4.4.9.2, sys clock 32 kHz	±10%	12.5		100	Hz
Sampling rate	4 steps, chapter 4.4.2, sys clock 32 kHz	±10%	125		1000	Hz
Clock						
System clock frequency	Over operating voltage and temperature		30.5		33.5	kHz
Clock frequency drift				100	200	ppm

*Maximum current is obtained at 85 °C, due to leakage current, these number is much higher than the typical current.
**Typical current is obtained at 27 °C.
***Tolerance at 30 °C.

4 Theory of Operation

The ASIC is the main part of InfraTec's digital pyroelectric detectors. It combines the essential signal processing steps of the pyroelectric signal from the amplification to the analog to digital conversion.

Chapter 4.1 gives an overview of the available pins of the ASIC. Note that not all pins of the ASIC may be accessible on your specific detector with digital communication interface. Please refer to the according data sheet for more information.

The working principle of the ASIC can be divided into different function blocks which are described in the following chapters:

- Analog section (chapter 4.2),
- Analog to digital converter (chapter 4.3),
- Digital section (chapter 4.4).

4.1 Pin Description

The functionality of the ASIC determines the functionality of the detector. Depending on the detector type, different function pins of the ASIC are routed to the detector pins. To get your specific detector pin configuration please refer to the data sheet of the detector. The following table gives an overview of the available function pins of the ASIC. A detailed description of the pin functions can be found in chapter 4.4.

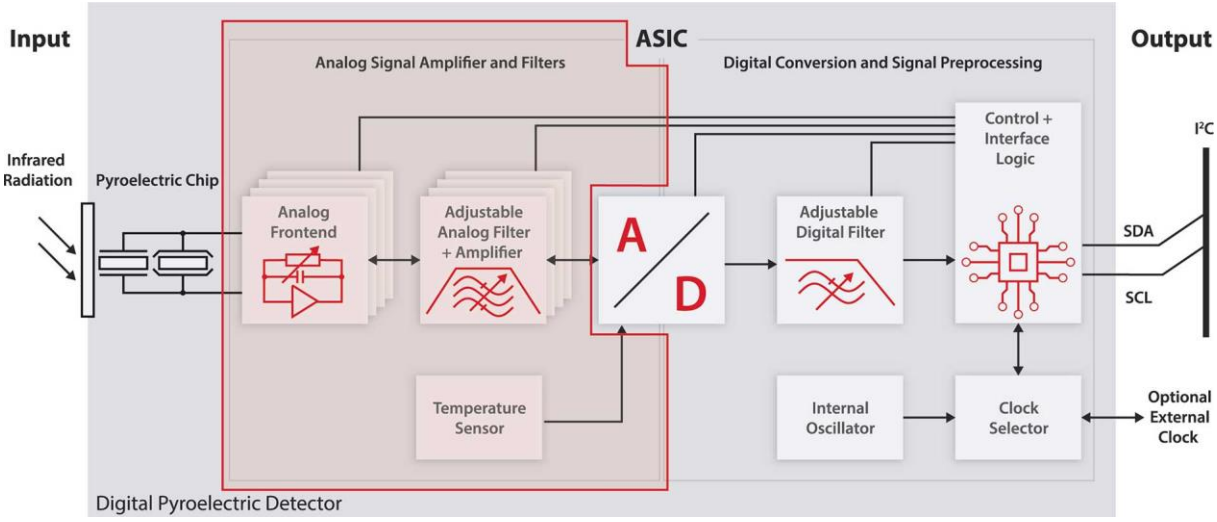
Pin	Description	Type	Comment	Detailed description
Vcc	Power Supply	Power	Mandatory	-
GND	Ground	Ground	Mandatory	-
SDA	I^2C data line*	Digital In / Out	Mandatory	Chapter 4.4.9
SCL	I^2C clock line*	Digital In	Mandatory	Chapter 4.4.9
CLK	ASIC clock frequency**	Digital In / Out	Optional	Chapter 4.4.4.1
INT	Interrupt	Digital Out	Optional	Chapter 4.4.8
SYNC	Synchronization signal	Digital In / Out	Optional	Chapter 4.4.4.2
PD	Power down	Digital In	Optional	Chapter 4.4.5

Table 1: ASIC pin functions

*This pin requires a pull-up resistor.

**The ASIC is designed to work with a 32 kHz clock. Many of detector parameters such as the feedback resistance, the sampling frequency and filter properties are derived from this main clock. It is essential that the clock is as precise and stable as possible.

4.2 Analog Section



Changes in the incoming IR-radiation lead to temperature changes of the pyroelectric chip which consequently result in a small electric current in the range of a few picoamps. Because of the high output impedance of the pyroelectric material the signal cannot be used directly for evaluation purposes. The analog front-end contains the required signal processing in form of a transimpedance amplifier.

4.2.1 Analog Front-End

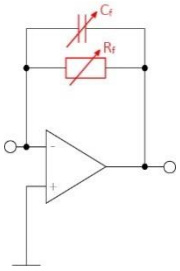


Figure 2: Analog front-end with transimpedance amplifier

The current generated by the sensor material is compensated by a transimpedance amplifier (TIA). As a result, the current flowing at the output of the low noise OpAmp is the same as the short-circuit current of the pyroelectric element which causes a voltage drop across the feedback path. To prevent any gain peaking and thus oscillation of the OpAmp, an additional capacitance is necessary in the feedback path. The combination of the capacitance and the resistance in the feedback network forms a low pass filter.

The most important features for characterizing the performance of a pyroelectric detector are the frequency-dependent sensitivity, noise density and detectivity D*. Depending on the measurement system and principle, there are different requirements for well-dimensioned signal processing. The ASIC offers full flexibility in the configuration of the detector parameters, during development as well as in later use. The sensitivity of the detector can be adjusted depending on the radiated power impinging the pyroelectric chip, in order to optimally utilise the subsequent input voltage range of the A/D converter. Feedback resistance R_f and feedback capacitance C_f can be set individually for each spectral channel of the detector. This allows the user to optimally adapt the performance of sensitivity and stability to the requirements of the application. The selectable values of the feedback resistance and capacitance can be found in the register map of the ASIC in chapter 4.4.9.2.

4.2.2 Analog Filter and Amplification Stage

As shown in Figure 1, the amplification of the small pyroelectric sensor signal in the analog front-end is followed by a first order band pass filter. The high pass cut-on frequency can be adjusted in the range of 0.5 – 4 Hz. Table 13 in chapter 4.4.9.2 shows all the possible configurations of the high pass filter. This high pass is superposed with the high pass characteristic of the pyroelectric chip.

The low pass cut-off frequency is 200 Hz and cannot be modified. Notice that there is an additional low pass filter in the digital part of the signal path which can be modified by the user (see chapter 4.4.1).
Further to the band pass filtering this stage allows the user to implement certain gain factors, which are listed in Table 3. This amplification stage enables the user to take full advantage of the whole ADC input range of 1.6 V.

4.2.3 Saturation Handling

Due to conditions such as external mechanical or thermal shocks, the generated current of the pyroelectric material can potentially reach levels that saturate the transimpedance amplifier in the analog front-end. This saturation, particularly with an unfavorable filter configuration, may result in a prolonged recovery time, possibly taking seconds. To address this, a fast reset circuit has been integrated to shorten the recovery time.

The fast reset circuit is triggered either when the analog front-end or the ADC operates beyond its standard range for a minimum of 128 clock cycles. For the analog front-end, the signal is considered outside the operating range when it deviates approximately ±5% from the rails, corresponding to 0.08 V to 1.52 V. On the other hand, for the ADC, the fast reset is activated when the signal is outside of 3.125 % to 96.875 % of the 16 bits. Table 2 sums up the different thresholds of the fast reset circuitry:

	Analog front-end	**ADC**
Low trigger level in counts	8,297	2,048
High trigger level in counts	57,918	63,488

Table 2: Thresholds for the fast recovery after saturation feature

Keep in mind that the threshold values can differ due to tolerance-related fluctuations of the internal ASIC components.

Once triggered, the fast reset remains active for 2048 clock cycles, equivalent to 64 ms, after the saturation event concludes. The fast reset is implemented as follows:

- The transimpedance feedback resistor will be reduced to 2 GΩ (lowest value),
- The high pass filter is set to 4 Hz cut-on frequency,
- Once the fast reset has ended, the circuit will go back to the previous setting,
- The fast reset will be also activated for 2048 clock cycles after a channel is enabled (64 ms). This will improve the start-up time of each channel.

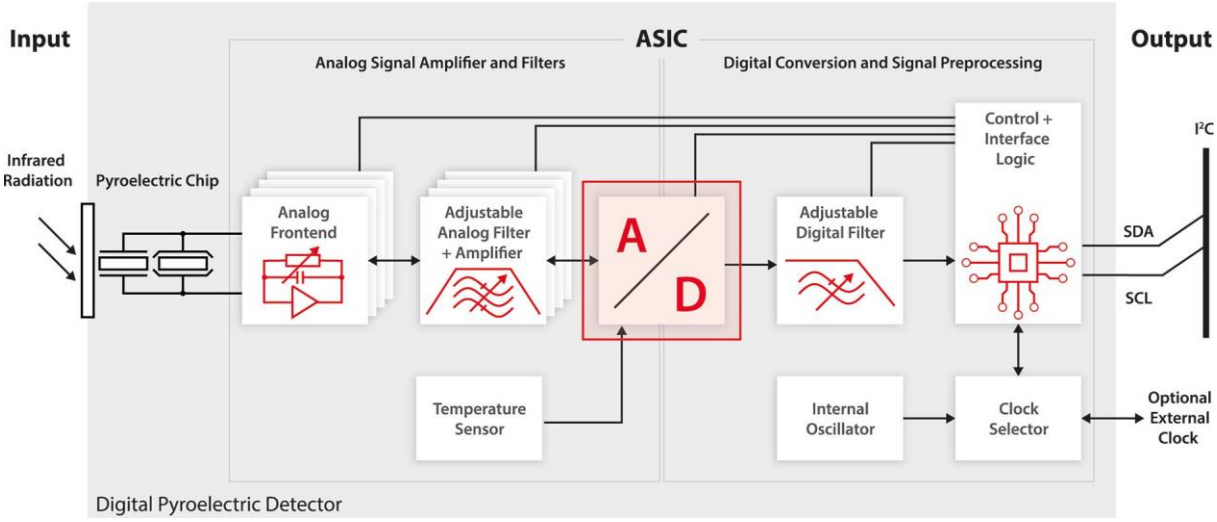
4.2.4 Temperature Sensor

The temperature is derived from the voltage drop across a pn-junction. This voltage will be converted into a digital code. The temperature resolution is 0.0121 K/count. The following formula can be used to calculate the temperature in degrees from the digital value:

$$\text{Temperature} / °C = \ 0.0121\ (x - 625) - 515$$

where x is the ADC counts.
Note that the calibration point is 30 °C with an absolute tolerance of ± 0.5 °C. The temperature readout at registers 0x09 and 0x0A is affected by an offset generated by the temperature calibration registers 0x21 and 0x22. The gain error is not quantified and can vary due to process variations.

4.3 Analog to Digital Converter



The next step after the analog section is the analog-to-digital conversion. The analog-to-digital converter (ADC) has a resolution of 16 bits, ensuring that the introduced quantization error remains significantly below the noise density of the analog front-end. Consequently, the final signal-to-noise ratio (SNR) of the system is determined by the performance of the analog front-end and is not limited by the capabilities of the ADC.

Apart from the gain controlled by the transimpedance amplifier and the gain of the previous band pass filter stage, the channel gain can also be adjusted by another gain stage in the ADC. The gain step is designed to have a continuous logarithmic step size from 0 dB to 22.5 dB (respectively 13.44 V/V). This gain amplifies both the signal and the noise hence the SNR does not improve. The gain of the filter and the ADC combined yield a total gain as shown in the following table:

Gain setting	Band pass gain in dB	ADC gain in dB	Total gain in dB	Total gain factor
0	0	0	0	1.00
1	1.5	0	1.5	1.19
2	3	0	3	1.41
3	4.5	0	4.5	1.68
4	0	6	6	2.00
5	1.5	6	7.5	2.37
6	3	6	9	2.81
7	4.5	6	10.5	3.35
8	0	12	12	3.98
9	1.5	12	13.5	4.73
10	3	12	15	5.62
11	4.5	12	16.5	6.68
12	0	18	18	7.94
13	1.5	18	19.5	9.44
14	3	18	21	11.22
15	4.5	18	22.5	13.34

Table 3: Resulting gain from band pass and ADC amplification stage

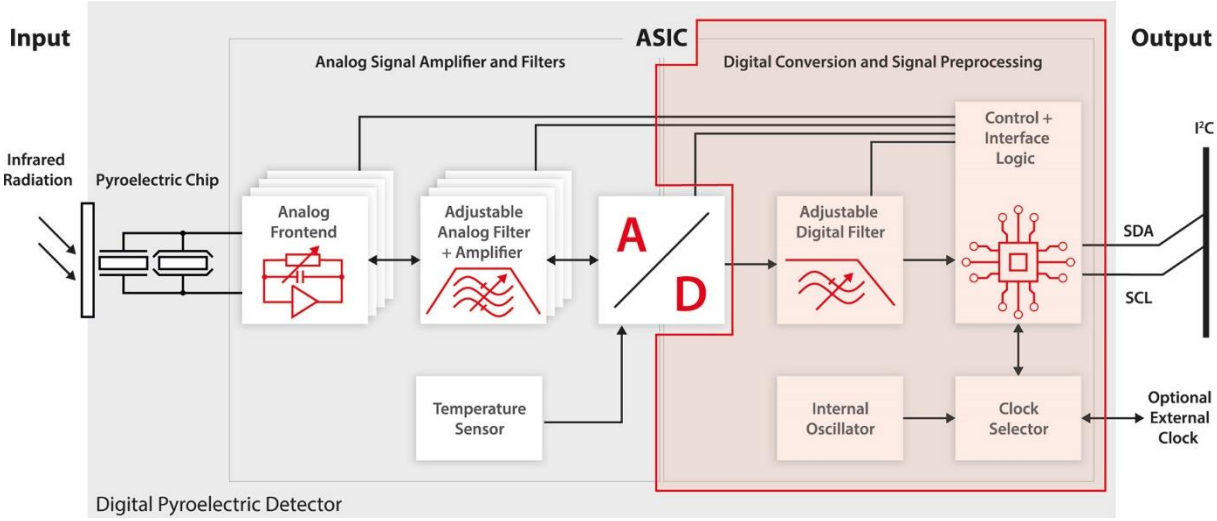
4.3.1 Conversion to Volts

To assess the performance of pyroelectric detectors, various sensor parameters are considered, with key metrics including responsivity, noise density and detectivity. Analog detectors typically measure responsivity and noise density in units of V/W and µV/√Hz, respectively. In the case of PyrIQ detectors, the analog-to-digital conversion already takes place in the ASIC and the measured values in counts can be read out via the digital interface. With formula (1) the digital signal values can be converted back to the corresponding voltages to calculate the sensitivity or noise density and compare the digital detectors with the analog ones.

$$U_{Volt} = 0.8\,V - (32{,}768 - Counts) \cdot U_{LSB} \qquad (1)$$

Here, U_{Volt} represents the signal in volts, Counts is the digital signal and U_{LSB} denotes the least significant bit voltage, which is 29.423 µV. The internal reference voltage of the analog front-end is 1.6 V. This yields in the offset of 0.8 V.

4.4 Digital Section



The ADC provides a 16 bits wide data word for each of the 5 channels (four sensor channels and one temperature channel) at a maximum sampling rate of 1 kHz. The signal chain inside the digital section is illustrated in the graph below.

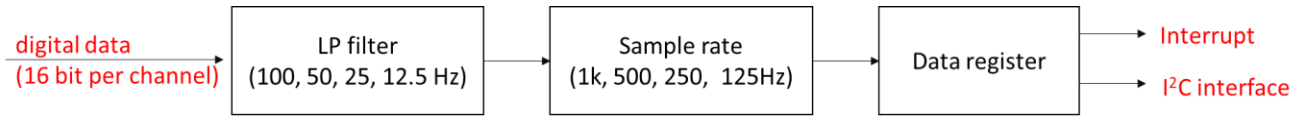


Figure 3: Digital signal chain for one channel

After the adjustable low pass filter there is a circuit which controls the sampling rate. Eventually, the values are stored in the data register. This register can be read by the user via the I²C interface. Moreover, after every write event an interrupt controller generates an interrupt. Due to the low pass filter between 12.5 – 100 Hz the detector with digital interface can only be used up to modulation frequencies of approximately 100 – 200 Hz.

The digital section offers a broad variety of adjustable features which are described in the following chapters 4.4.1 - 4.4.9. As mentioned in 4.1, not all available function pins of the ASIC may be present in your specific detector. Please refer to the data sheet of the detector for the available pin functions.

4.4.1 Digital Filter Stage

The output of the ADC is followed by a programmable first order low pass filter. This filter stage removes unwanted high frequencies. The available cut-off frequencies are 100, 50, 25 and 12.5 Hz and can be modified as described in chapter 4.4.9.2.

4.4.2 Sampling Rate Control

The input frame rate is at 1 kHz, while the output frame rate can be divided down to 1 kHz, 500 Hz, 250 Hz and 125 Hz. At a frame rate less than 1 kHz, the output data will be an average of all the data during that frame as shown in Table 4.

Sampling Rate	**Output** {x} = Value of Frame x							
@1 kHz	{1}	{2}	{3}	{4}	{5}	{6}	{7}	{8}
@ 500 Hz	avg ({1}, {2})		avg ({3}, {4})		avg ({5}, {6})		avg ({7}, {8})	
@ 250 Hz	avg ({1}, {2}, {3}, {4})				avg ({5}, {6}, {7}, {8})			
@ 125 Hz	avg ({1}, {2}, {3}, {4}, {5}, {6}, {7}, {8})							

Table 4: Effect of the selected sampling rate to the output value

4.4.3 Data Register

At the end of each conversion process the digitalized data of all four channels and the temperature sensor are written into the data register. This register can be read out via the I^2C interface. The exact memory space of the data can be inferred from Table 6 in chapter 4.4.9.2. Note that the register channel of the sensor data may not match with the optical channel of the detector. The conjunction between the sensor input channel of the ASIC (respectively the data register) and the channel number of the detector is presented in the detector data sheet.

4.4.4 Synchronization

For precise measurement results with a pulsed IR-source as e.g., used in NDIR gas measurement systems, it may be important that the excitation signal and the sampling process are synchronized. This approach allows the exact determination of the RMS value of the fundamental wave. Synchronization in this context especially means that the phase between the IR-source and the sampling process is locked. The absolute phase between the two signals is not as significant as the locked phase because it does not change the RMS of the signal. A locked phase can be realized when the clock rate of the ASIC and the clock rate of the modulation frequency are derived from the same clock source.

To implement a synchronization mechanism the ASIC offers the two pins CLK and SYNC. The configuration of these pins is controlled by SYS_CFG register bits [3:2] (SYN_SRC and CLK_SRC, see chapter 4.4.9.2). The selection will affect the behavior of the pins CLK and SYNC which can serve either as digital input or output. The CLK pin is crucial for a locked phase whereas the SYNC pin controls the phase position. If the internal clock of the ASIC and the clock of the excitation signal operate independently from each other, the phase between the signals will change over time which may have a small effect on the derived RMS value.

4.4.4.1 Clock Selection

By default, the internal clock is used (32 kHz) and the clock output will appear on the CLK pin (if the clock output is enabled at bit 4 of SYS_CFG). If the external clock is selected, the IC expects an external clock on pin CLK as an input. Note that a lot of detector parameters such as the feedback resistance, the sampling frequency and filter properties are frequency dependant. Their operation will change with the clock frequency. The parameter configuration described in chapter 4.4.9.2 refers to a clock frequency of 32 kHz.

4.4.4.2 Sync Selection

The SYNC pin can also be configured as output or input. In the first case the ASIC will output a 1 kHz signal with a pulse width of four clock cycles (125 µs @ 32 kHz system clock) at the SYNC pin. The ADC data will be available at the falling edge of the SYNC signal. This option can be used analogous to an interrupt-based system (see chapter 4.4.8).

In the second case a rising edge at the SYNC pin will cause the state machine of the ADC to reset. This will start a new sampling procedure. Hence this enables the user to start the conversion at a well-defined point of time with respect to the excitation signal. Valid data will be available after between 546 and 770 clock cycles, depending on the sampling rate. When the pin is configured as input it is recommended to not leave the pin floating.

Sampling Rate in Hz	Data valid	
	Clock cycles	Time in ms @ 32 kHz system clock
1000	546	16
500	578	18
250	642	20
125	770	24

Table 5: Valid data after external SYNC event

4.4.5 Power Management

Note: The PD pin must be pulled down to GND to enable the detector (if PD pin is available as a detector pin).
To optimize the power consumption, each analog channel can be turned on / off independently. To power down the ASIC, the user can either pull the PD pin to high (3.3V) or set bit SLEEP_EN in the SYS_CFG register. The PD pin will also act as a reset pin and will reset all the internal registers to their respective default value. When using the SLEEP_EN functionality the device will keep its internal register configuration.
Furthermore, the power consumption can be optimized by switching off unused ASIC input channels with the MODE bit in the corresponding ASIC configuration register. Refer to 4.4.9.2 for more information.

4.4.6 Start-Up

When PD goes from high to low, the oscillator will start, and the internal reset will be released after 64 clock periods. The I^2C interface is responsive before the start-up time has ended but the retrieved data may not be accurate. For valid data it is obligatory to wait for 2048 clock periods respectively 64 ms.
After the internal reset is released, the ASIC reads the One Time Programmable (OTP) Memory for 325 clock cycles. The start-up sequence will last less than 512 clock periods from the falling edge of PD.

4.4.7 One Time Programmable Memory

The OTP contains calibration data for the internal oscillator and the integrated temperature sensor. These three bytes are protected with a checksum. During the start-up this checksum is evaluated. If it is valid, the OTP data is used, if the checksum is not valid, default values will be used. For more details refer to the register map in chapter 4.4.9.2 and the bits OTP_SEQ[3:2] in the STATUS register.

Additionally, the OTP also holds six identification bytes which contain a unique lot number of the according ASIC, the wafer number and the coordinates at the wafer. The OTP data cannot be read out directly like the other I^2C register data. Instead, the following procedure must be applied:

- Enable the OTP read by setting OTP_RD_EN (bit 2 of OTP_CFG register, address 0x14),
- Wait for at least 325 clock periods,
- Read I^2C register 0x01 to 0x0a for the corresponding 10 OTP bytes,
- Reset OTP_RD_EN for reading sensor data.

4.4.8 Interrupt and Overwritten Flag

Depending on the sampling rate selection, the interrupt line (active low) will go down when new data is ready. The interrupt will be reset after an I²C-read-sequence from any of the memory data space (0x01 to 0x0A). The INT bit in the STATUS register behaves like the interrupt output pin. Refer to chapter 4.4.9.2 for more information.
When a new data set is ready and the old data is not read yet, bit OVW in the STATUS register (0x00) will be set. It will be reset once data is read. It is recommended to leave the INT pin floating.

4.4.9 I²C Interface

The device acts as an I²C slave device with a 7-bit device address protocol. The SCL line will be always an input, while the SDA line is configured as an open drain driver with an internal 50 kΩ pull up, which is compatible with 8 kbit/s data rate. For faster access speed, up to 1000 kbit/s, a smaller external Pull-Up resistor is required (typically 1 kΩ).
A typical I²C frame is given below. The read and write sequences are described in chapter 4.4.9.3. The ASIC is not compatible with the clock stretching feature.

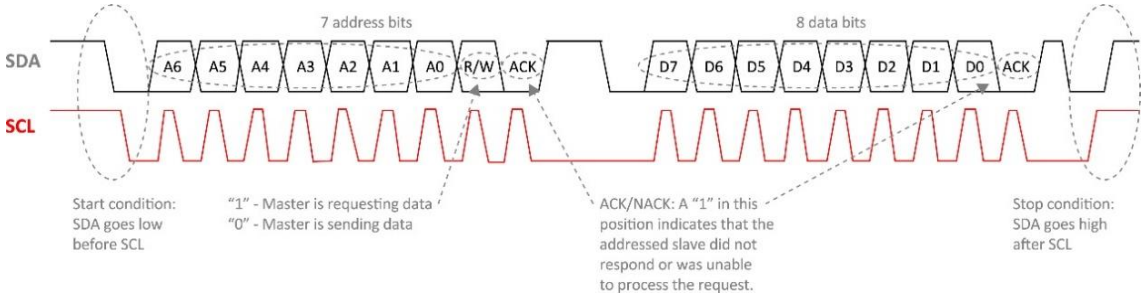


Figure 4: Typical I²C frame

The digital interface of the detector supports Fast Mode Plus (FM+) with clock rates up to 1 MHz. The configured clock speed should also be selected regarding the capacity of the bus and the used pull-up resistors. Pivotal for the applicable bandwidth is the time constant of the RC-network consisting of the bus capacity and the pull-up resistors. E.g., long wires of the I²C lines require smaller pull-up resistors so that the consequential time constant is low enough to meet the I²C rise time specifications. The FM+ for instance requires a maximum rise time to the detection threshold as fast as 120 ns. The decision for the resistance of the pull-up should also be based on the power budget as smaller resistors yield a higher power consumption.

4.4.9.1 Addressing

The default I²C address for the device is 0x5a and can be changed to any valid address by writing into the register at address 0x15.

When the user wants to use multiple detectors on one I²C bus, it is mandatory that each device has its unique I²C address. Therefore, the devices need to be powered-up in sequence to give each one an exclusive address.

4.4.9.2 Register Map

Register-ID	Address	Mode	Bit position							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS	0x00	R	SAT4	SAT3	SAT2	SAT1	OTP_SEQ [3:2]		OVW	INT
S1_H	0x01	R	DATA_H [15:8]							
S1_L	0x02	R	DATA_L [7:0]							
S2_H	0x03	R	DATA_H [15:8]							
S2_L	0x04	R	DATA_L [7:0]							
S3_H	0x05	R	DATA_H [15:8]							
S3_L	0x06	R	DATA_L [7:0]							
S4_H	0x07	R	DATA_H [15:8]							
S4_L	0x08	R	DATA_L [7:0]							
T_H	0x09	R	TEMP_DATA_H [15:8]							
T_L	0x0a	R	TEMP_DATA_L [7:0]							
S1_CFGa	0x0b	R/W	MODE	FB_RES [6:3]				FB_CAP [2:0]		
S1_CFGb	0x0c	R/W	HP_FLT [7:6]		LP_FLT [5:4]		ADC_GAIN [3:2]		BP_GAIN [1:0]	
S2_CFGa	0x0d	R/W	MODE	FB_RES [6:3]				FB_CAP [2:0]		
S2_CFGb	0x0e	R/W	HP_FLT [7:6]		LP_FLT [5:4]		ADC_GAIN [3:2]		BP_GAIN [1:0]	
S3_CFGa	0x0f	R/W	MODE	FB_RES [6:3]				FB_CAP [2:0]		
S3_CFGb	0x10	R/W	HP_FLT [7:6]		LP_FLT [5:4]		ADC_GAIN [3:2]		BP_GAIN [1:0]	
S4_CFGa	0x11	R/W	MODE	FB_RES [6:3]				FB_CAP [2:0]		
S4_CFGb	0x12	R/W	HP_FLT [7:6]		LP_FLT [5:4]		ADC_GAIN [3:2]		BP_GAIN [1:0]	
SYS_CFG	0x13	R/W	SMP_FRQ [7:6]		I2C_ PULL	CLK_ OUT	SYNC_ SRC	CLK_ SRC	SLEEP_ EN	INT_ EN
OTP_CFG	0x14	R/W	-				OTP_ BYPSS	OTP_R D_EN	-	
I2C_ADD	0x15	R/W	BIT0_ DEV	DEV_ADDR [6:0]						
OSC_CAL	0x20	R	-	OSC_CAL_DATA [6:0]						
T_CAL_H	0x21	R	TEMP_CAL_DATA_H [7:0]							
T_CAL_L	0x22	R	TEMP_CAL_DATA_L [7:0]							
CHK_SUM	0x23	R	CHK_SUM_DATA [7:0]							
SERIAL_ID	0x24	R	LOT_BYTE_0 [7:0]							
SERIAL_ID	0x25	R	LOT_BYTE_1 [7:0]							
SERIAL_ID	0x26	R	LOT_BYTE_2 [7:0]							
SERIAL_ID	0x27	R	WAFER_NUM [7:0]							
SERIAL_ID	0x28	R	WAFER_X_COORD [7:0]							
SERIAL_ID	0x29	R	WAFER_Y_COORD [7:0]							

Table 6: Register map

Note: The register channel of the sensor data may not match with the optical channel of the detector. The assignment between the sensor input channel of the ASIC (respectively the data register) and the channel number of the detector is presented in the detector data sheet.

INT **@ STATUS 0x00**

The interrupt flag INT acts like the interrupt output pin of the ASIC. The INT bit is set to low when new data is available. It is set to high when the host is reading any of the memory data space (0x01 to 0x0A). E.g., when the host is reading the same data twice, the second read INT bit will be high.

OVW **@ STATUS 0x00**

When a new data set is ready and the old data is not read yet, the overwritten flag OVW will be set to high. It will be reset once data is read.

OTP_SEQ [3:2] **@ STATUS 0x00**

If the first bit OTP_SEQ [2] is high, the OTP read was completed. If this bit is low the read was not done (e.g., if you bypass the calibration with the OTP data by setting OTP_BYPSS at register OTP_CFG). Bit OTP_SEQ [3] indicates if the read data is valid (bit is one) or not (bit is zero).

SAT1, SAT2, SAT3, SAT4 **@ STATUS 0x00**

These registers are set to one when the corresponding ASIC channel is saturated. The saturation condition is fulfilled when the output of the transimpedance amplifier in the analog front-end is saturated or the ADC is outside its normal operating range (6% - 94%) for a minimum of 128 clock cycles.

DATA_H **@ S1_H 0x01, S2_H 0x03, S3_H 0x05, S4_H 0x06**

DATA_H is the high data byte of the corresponding sensor input channel. Together with the low data byte DATA_L these registers build the 16 bit digital value of the sensor input channel. Depending on the detector configuration, not all sensor input channels are connected to a pyroelectric chip.

DATA_L **@ S1_H 0x02, S2_H 0x04, S3_H 0x06, S4_H 0x08**

DATA_L is the low data byte of the corresponding sensor input channel. Together with the high data byte DATA_H these registers build the 16 bit digital value of the sensor input channel. Depending on the detector configuration, not all sensor input channels are connected to a pyroelectric chip.

FB_CAP [2:0], default 0x04 **@ S1_CFGa 0x0b, S2_CFGa 0x0d, S3_CFGa 0x0f, S4_CFGa 0x11**

These bits control the value of the feedback capacitor as described in Table 7. Every channel has its own feedback network. Thus, the feedback capacitance can be set for each channel individually. Refer to chapter 4.2.1 for more information.

Register value	Feedback capacitance in fF
0b000	50
0b001	100
0b010	200
0b011	400
0b100	800
0b101	1600
0b110	3200
0b111	6400

Table 7: FB_CAP options

FB_RES [6:3], default 0x04 **@ S1_CFGa 0x0b, S2_CFGa 0x0d, S3_CFGa 0x0f, S4_CFGa 0x11**

These bits control the feedback resistance as described in Table 8. Every channel has its own feedback network. Thus, the feedback resistance can be set for each channel individually. Refer to chapter 4.2.1 for more information.

Register value	Feedback resistance in GΩ
0b0000	2
0b0001	4
0b0010	8
0b0011	16
0b0100	32
0b0101	64
0b0110	128
0b0111	256[1]
0b1000	512[1]
0b1001	1024[1]

Table 8: FB_RES options

MODE, default 0x00 **@ S1_CFGa 0x0b, S2_CFGa 0x0d, S3_CFGa 0x0f, S4_CFGa 0x11**

To optimize the power consumption, each analog input channel can be turned on / off independently via the MODE register. Refer to chapter 4.4.5 for more information.

Register value	Meaning
0b0	The according sensor input is turned on.
0b1	The according sensor input is turned off

Table 9: MODE options

BP_GAIN [1:0], default 0x00 **@ S1_CFGb 0x0c, S2_CFGb 0x0e, S3_CFGb 0x10, S4_CFGb 0x12**

These bits control the band pass gain after the analog front-end. Refer chapter 4.2.2 for more information.

Register value	Band pass gain in dB
0b00	0.0
0b01	1.5
0b10	3.0
0b11	4.5

Table 10: BP_GAIN options

ADC_GAIN [3:2], default 0x00 **@ S1_CFGb 0x0c, S2_CFGb 0x0e, S3_CFGb 0x10, S4_CFGb 0x12**

These bits control the ADC gain. Refer to chapter 4.3 for more information.

Register value	ADC gain in dB
0b00	0
0b01	6
0b10	12
0b11	18

Table 11: ADC_GAIN options

[1] Due to the realization of these resistances these configurations only increase the responsivity. The SNR does not improve compared to the 128 GΩ resistance.

LP_FLT [5:4], default 0x00 **@ S1_CFGb 0x0c, S2_CFGb 0x0e, S3_CFGb 0x10, S4_CFGb 0x12**

These bits control the low pass filter cut-off frequencies after the ADC. Refer to chapter 4.4.1 for more information.

Register value	Low pass cut-off frequency in Hz
0b00	100.0
0b01	50.0
0b10	25.0
0b11	12.5

Table 12: LP_FLT options

HP_FLT [7:6], default 0x00 **@ S1_CFGb 0x0c, S2_CFGb 0x0e, S3_CFGb 0x10, S4_CFGb 0x12**

These bits control the high pass filter cut-on frequencies before the ADC. Refer to chapter 4.2.2 for more information.

Register value	High pass cut-on frequency in Hz
0b00	0.5
0b01	1.0
0b10	2.0
0b11	4.0

Table 13: HP_FLT options

INT_EN, default 0x01 **@ SYS_CFG 0x13**

INT_EN controls the INT pin of the IC.

Register value	Meaning
0b0	Interrupt at INT pin of ASIC and INT bit in STATUS register are disabled.
0b1	Interrupt at INT pin of ASIC and INT bit in STATUS register are enabled.

Table 14: INT_EN options

SLEEP_EN, default 0x00 **@ SYS_CFG 0x13**

With SLEEP_EN the device can be sent to sleep mode while keeping its internal register configuration. More information can be found in chapter 4.4.5.

Register value	Meaning
0b0	Device is on.
0b1	Device is in sleep mode.

Table 15: SLEEP_EN options

CLK_SRC, default 0x00 **@ SYS_CFG 0x13**

CLK_SRC determines the clock source. For more information see chapter 4.4.4.1.

Register value	Meaning
0b0	The internal oscillator is used as ASIC clock.
0b1	The supplied clock at the CLK pin is used as ASIC clock.

Table 16: CLK_SRC options

SYNC_SRC, default 0x00 @ SYS_CFG 0x13

SYNC_SRC controls the SYNC pin of the ASIC. A detailed description can be found in chapter 4.4.4.2.

Register value	Meaning
0b0	Sets synchronization mode to internal. The SYNC pin is set as an output pin. ADC data will be available at the falling edge of the SYNC signal. Pulse width is four clock cycles.
0b1	Sets synchronization mode to external. The SYNC pin is set as an input pin. The rising edge of the SYNC causes the state machine of the ADC to reset.

Table 17: SYNC_SRC options

CLK_OUT, default 0x00 @ SYS_CFG 0x13

Controls the CLK pin of the ASIC. See chapter 4.4.4.1 for more information. The clock output is only valid if the clock source @ CLK_SRC is set to internal.

Register value	Meaning
0b0	The output of CLK pin is disabled hence it can be used as input.
0b1	The clock of the internal oscillator is output at the CLK pin.

Table 18: CLK_OUT options

I2C_PULL, default 0x00 @ SYS_CFG 0x13

With I2C_PULL the internal pull-up for the I^2C interface can be controlled.

Register value	Meaning
0b0	Enable internal I^2C pull-up. The resistance of the pull-up is approximately 50 kΩ.
0b1	Disable internal I^2C pull-up.

Table 19: I2C_PULL options

SMP_FRQ [7:6], default 0x03 @ SYS_CFG 0x13

This register controls the sampling frequency as described in Table 20. More Information is provided in chapter 4.4.2.

Register value	Sampling frequency in Hz
0b00	1000
0b01	500
0b10	250
0b11	125

Table 20: SMP_FRQ options

OTP_RD_EN, default 0x00 @ OTP_CFG 0x14

Set bit high to read the data inside the OTP Memory. After setting the bit and waiting at least 325 clock cycles the OTP data can be read from the I^2C registers 0x01 – 0x0a. Refer to chapter 4.4.7 for more information.

OTP_BYPSS, default 0x00 @ OTP_CFG 0x14

Set bit high to bypass the data of the OTP Memory. Please note that it is not recommended to bypass the data of the OTP as they are used to calibrate the temperature and internal 32 kHz clock.

DEV_ADDR [6:0], default 0x5a @ I2C_ADD 0x15

DEV_ADDR contains the I^2C device address of the ASIC which can be changed by the host.

BIT0_DEV, default 0x00 **@ I2C_ADD 0x15**

BIT0_DEV defines if bit 0 of register I2C_ADD @ 0x15 is set by an external pin of the ASIC or if the internal register is used. Refer to chapter 4.4.9.1 for more information.

Register value	Meaning
0b0	Use external pin for bit 0 of DEV_ADDR.
0b1	Use register value for bit 0 of DEV_ADDR.

Table 21: BIT0_DEV options

Note: To read out registers 0x20 – 0x29 you must set the read enable bit OTP_RD_EN (bit 2 of OTP_CFG register) and wait at least 325 clock cycles. Afterwards you can readout the OTP data at the I2C registers 0x01 – 0x0a. To read sensor values you must set bit OTP_RD_EN to low.

OSC_CAL_DATA [6:0] **@ OSC_CAL 0x20**

This register contains the calibration data for the internal oscillator.

T_CAL_DATA_H [7:0] **@ T_CAL_H 0x21**

This register holds the high data byte of the calibration data for the integrated temperature sensor.

T_CAL_DATA_L [7:0] **@ T_CAL_L 0x22**

This register holds the low data byte of the calibration data for the integrated temperature sensor.

CHK_SUM_DATA [7:0] **@ CHK_SUM 0x23**

This register contains the checksum of the registers OSC_CAL_DATA, T_CAL_DATA_H and T_CAL_DATA_L. The OTP data is considered valid if the sum of the three bytes equals a certain calculated value. This value is calculated by adding the three bytes and inverting the result.
E.g., if all 3 bytes are zero the checksum is 0xff. If all bytes are 0xff, the sum of them is 0b10 111 1101. Because the checksum only is one byte wide the resulted checksum is 0b10 respectively 0x02.

LOT_BYTE_0 [7:0] **@ SERIAL_ID 0x24**

This register contains the LSB of the three-byte wide ASIC specific lot number.

LOT_BYTE_1 [7:0] **@ SERIAL_ID 0x25**

This register contains the second of the three-byte wide ASIC specific lot number.

LOT_BYTE_2 [7:0] **@ SERIAL_ID 0x26**

This register contains the MSB of the three-byte wide ASIC specific lot number.

WAFER_NUM [7:0] **@ SERIAL_ID 0x27**

This register holds the wafer number of the according ASIC.

WAFER_X_COORD [7:0] **@ SERIAL_ID 0x28**

This register holds the x-coordinate at the wafer of the according ASIC.

WAFER_Y_COORD [7:0] **@ SERIAL_ID 0x29**

This register holds the y-coordinate at the wafer of the according ASIC.

4.4.9.3 Command Sequence

Note that the I²C interface allows continuous reading from the register of the ASIC.